Recently, a so-called damascene process has been adopted to provide multilevel interconnections for a semiconductor device having a metal or conductive film buried in the insulating film.

At page 1, replace the paragraph beginning at line 22 with the following:

It is known that, where the conductive film 5 is removed by the CMP process, as the opening area of the trench increases, the polish rate on the conductive film buried in the trench increases, as shown in Figure 2. In regions having a small trench opening area, such as is customary in interconnections, there are no particular problems. However, in regions having a large trench opening area, such as a bonding pad 6 shown in Figure 3, the conductive film 5 in the trench is polished into a dish-like form by an abrasive as shown in Figure 4, thus resulting in so-called dishing. Due to this, there are cases a disconnect or an increase of resistance occurs in a central portion A where the wall thickness is reduced when providing connection between the bonding pad and the IC frame.

B1

At page 2, replace the paragraph beginning at line 11 with the following:

Another object of the invention is to provide a damascene interconnection capable of preventing increases in resistance value or disconnects caused by dishing in a bonding pad, and a semiconductor device using the same.

B2

At page 3, replace the paragraph beginning at line 2 with the following:

When removing the conductive film by a CMP process or the like, the protrusion dividing the pad trench serves as a stop for polishing by an abrasive. Consequently, so-called dishing will not occur such that the conductive film in the pad trench is excessively removed. Thus, according to the invention, it is possible to prevent increases in resistance or disconnects resulting from dishing on a bonding pad.

B3

At page 3, replace the paragraph beginning at line 21 and ending at page 4, line 11 with the following:

Figure 1 is an illustrative view showing a process for a general damascene interconnection;

Figure 2 is a graph showing a usual polish characteristic in CMP;

Figure 3 is an illustrative view showing a prior art bonding pad;

Figure 4 is a sectional view taken along line X-X in Figure 3;

Figure 5 is an illustrative view showing one embodiment of the present invention;

Figure 6 is a sectional view taken along line VI-VI in Figure 5;

Figure 7 is an illustrative view showing a method for forming the Figure 5 embodiment;

Figure 8 is an illustrative view showing another embodiment of the invention;

Figure 9 is an illustrative view showing another embodiment of the invention;

Figure 10 is an illustrative view showing another embodiment of the invention;

Figure 11 is a sectional view on line XI-XI in Figure 10;

Figure 12 is an illustrative view showing another embodiment of the invention; and

Figure 13 is an illustrative view showing another embodiment of the invention.

At page 4, replace the paragraph beginning at line 14 with the following:

A semiconductor device 10 of the embodiment shown in Figure 5 and Figure 6 includes a semiconductor substrate 12 formed, for example, of silicon (Si) or the like. Note that the semiconductor substrate 12 may be other materials. Semiconductor elements, including active and/or passive elements, are formed on the semiconductor substrate 12, although they are not shown in the figure.

At page 4, replace the paragraph beginning at line 19 with the following:

The semiconductor device 10 comprises a damascene interconnection 11 including, on the semiconductor substrate 12, an interconnection trench 16 extending from the semiconductor element (not shown) and a pad trench 18 connected to the interconnection trench 16. That is, an insulating film 14 is formed, for example, of silicon oxide (SiO_2) in a uniform film thickness on the semiconductor substrate. In the insulating film 14, the interconnection trench 16 and the pad trench 18 connected therewith are formed. The insulating film 14 may be other materials.

At page 5, replace the paragraph beginning at line 1 with the following:

Note that Figure 5 and Figure 6 illustrate the insulating film 14 formed directly on the surface of the semiconductor substrate 12 in order to simplify illustration and explanation. However, in the actual semiconductor device, one or a plurality of semiconductor element layers are formed on the semiconductor substrate 12, as is well known in the art, and an interconnection layer is formed as required on each of such semiconductor element layers. The interconnection trench 16 provides electrical connection between the semiconductor element (not shown) and the pad trench 18. The pad trench 18 serves as a bonding pad on which wire-bonding is to be made to a not-shown IC leadframe. That is, the pad trench 18 is a connection terminal to provide electric conduction of the semiconductor element on each layer to and from the IC leadframe.

At page 5, replace the paragraph beginning on line 15 with the following:

In this embodiment, however, the following devise is implemented on the pad trench 18 with a comparatively large opening area, in order to prevent dishing as stated before. That is, the pad trench 18 has an insulating film 14 formed to be left as an island-spotted form. Consequently, the pad trench 18 is divided into unitary portions by island protrusions 20. However, the island protrusions 20 do not separate one portion from another portion of the pad trench 18, i.e. the pad trench 18 is continuous in areas except for the island protrusions

cont. B8

20. That is, the pad trench 18 in this embodiment has a large opening size but is reduced in its substantial opening area by the presence of the island protrusions 20. Specifically, in this embodiment the pad trench 18 has a side determined as approximately 50 - 200 μm and an interval of the protrusions 20 determined as approximately 5 - 20 μm.

At page 6, replace the paragraph beginning on line 9 with the following:

B9

Hereunder, explanation is made on a method to concretely manufacture a semiconductor device 10 of the embodiment having a damascene interconnection 11 as described above, with reference to Figure 7. Incidentally, in Figure 7, an insulating film 14 is formed directly on a surface of a semiconductor substrate 12. It should however be noted that the semiconductor device 10, in practice, has a proper number of semiconductor element layers as stated before and Figure 7 depicts an interconnection structure having only one layer for the sake of convenience.

At page 6, replace the paragraph beginning on line 25 and ending at page 7, line 14 with the following:

B10

In the CMP process, the semiconductor substrate 12 (including the insulating film 14 and the conductive film 22) is urged onto a polishing pad mounted on a polisher table. The table and the substrate holder are relatively rotated while supplying to the polishing pad a slurry containing abrasive particles. When the conductive film 22 on the insulating film 14 is removed, the polishing operation is finished. In this case, the abrasive particle for polishing is selected of a kind (material, particle size, etc.) such that in CMP a polish rate on the insulating film 14 is lower than a polish rate on the conductive film 22. According to an experiment conducted by the present inventors, the polish rate in concrete is desirably given as (polish rate on the conductive film 22) / (polish rate on the insulating film 14) $\geq$ 20 to 10. This is because in CMP the conductive film 22 on the insulating film 14 needs to be removed as rapidly as possible. However, the insulating film 14 should be prevented from being damaged due to polishing, and the island projections 20 are to prevent over-polishing the

cont. B10

conductive film 22 of the pad trench 18. Consequently, there is a necessity of providing the insulating film 14 with greater polish resistance than that of the conductive film 22.

At page 7, replace the paragraph beginning on line 15 with the following:

B11

According to this embodiment, in the process of removing the conductive film 22 (Figure 7(d)), the protrusions 20 (insulating film 14) having a low polish rate act such that the conductive film 22 is decelerated during the process of polishing by the polish pad. Thus, the conductive film 22 in the pad trench 18 can be prevented from being removed to an excessive extent. This in turn makes it possible to prevent the pad trench 18 from increasing in resistance or the occurrence of disconnects due to dishing.

At page 7, replace the paragraph beginning on line 21 and ending at page 8, line 3 with the following:

B12

That is, in the conventional art shown in Figure 3 and Figure 4, because the pad trench 6 is contacted in its entire opening by a polish pad (not shown), the pad trench 6 having a large opening area is partly over-polished resulting in dishing. On the contrary, in this embodiment, despite the pad trench is large in an opening area, the opening is divided into unitary portions wherein the opening area is small if considered on a portion sandwiched between the island protrusions 20. Due to this, over-polish will not occur. As a result, a conductive film 22 in the pad trench 18 is given a planar surface as shown in Figure 6 and Figure 7(d).

At page 8, replace the paragraph beginning on line 4 with the following:

B13

In this manner, in the present invention, where using a CMP method having a polish characteristic that the polish rate increases with an increase in the opening area, the forming of protrusions in the pad trench reduces the substantial opening area, thereby preventing dishing.

At page 8, replace the paragraph beginning on line 11 with the following:

That is, in the embodiment shown in Figure 8, a plurality of protrusions or ridges 20 are formed extending from respective outer edges of four sides of a rectangular pad trench 18. It should be noted that, in also this case, the other areas of the pad trench 18 are continuous with one another. In also this embodiment, the substantial opening area is reduced in the areas between the protruding ridges 20, between protruding ridges extending from different sides, and between the protruding ridge 20 and the inner edge of the pad trench 18.

B14

At page 8, replace the paragraph beginning on line 18 with the following:

In the embodiment of Figure 9, a pad trench 18 has one ridge 20 formed in a squared-spiral form. In the Figure 9 embodiment, because the ridge 20 is in the spiral form, the pad trench 18 is not divided into non-continuous areas. In this manner, by forming the ridge 20 in the spiral form, the opening area is substantially reduced in the areas between portions of the ridge 20 and between the ridge 20 and the pad trench 18 inner edge.

B15

At page 9, replace the paragraph beginning on line 2 with the following:

Explanation is made in detail on an embodiment having contact holes 26 formed through the insulating film 14, with reference to Figure 10 and Figure 11. This embodiment is to be applied to a semiconductor device having another layer formed in a level lower than the insulating film 14, as shown in Fig. 11. That is, another insulating film 28 is formed on a semiconductor substrate 12, and further another conductive film 30 is formed on the insulating film 28. The insulating film 14 is formed on the conductive film 30. In a bottom of the pad trench 18, a plurality of contact holes 26 are formed penetrating through the insulating film 14. When forming a metal or conductive film 22 in the pad trench 18, a metal or conductive material thereof is also filled in the contact holes 26 to provide electrical connection between the upper-leveled conductive film 22 and lower-leveled conductive film

B16

cont. B16

30. By thus forming the contact holes 26 in the pad trench 18 and connecting the conductive films 22 and 30, it is possible to eliminate the disadvantage as feared upon forming protrusions 20 in the pad trench 18.

At page 9, replace the paragraph beginning on line 15 with the following:

B17

That is, the protrusions or ridges, if formed in the pad trench 18, result in a volume decrease of the pad trench 18, i.e. volume reduction of the conductive film 22 of the pad trench 18. It is to be feared that the bonding pad may be increased in electric resistance by the volume reduction in the conductive film 22 of the pad trench 18. However, the conductive film 22, if coupled to the conductive film 30 as in the Figure 10 and Figure 11 embodiments, increases the effective volume of the conductive film 22, thus properly suppressing the electric resistance from increasing.

At page 9, replace the paragraph beginning on line 25 and ending at page 10, line 11 with the following:

B18

In an embodiment of Figure 13, a ridge 20 is formed in a closed-loop form in a manner different from the Figure 9 embodiment. Accordingly, in this embodiment, the conductive film 22 of the pad trench 18 is divided into portions, in a manner different from the above embodiment. In this case, the contact holes 26 are especially effective. That is, the formation of contact holes 26 connects the conductive film 22 of the pad trench 18 to a lower-leveled conductive film 30 (Figure 11). Consequently, the divided portions of the conductive film 22 of the pad trench 18 are electrically coupled together through the conductive film 30. That is, in the Figure 13 embodiment, the ridge or protrusion 20 is formed in a closed-loop form. However, no problem is encountered with disconnects in the pad trench 18 due to the protrusion or ridge 20 because the conductive film 22 is coupled to the lower-leveled conductive film through the via holes 26.